REMARKS

The Office Action of August 11, 2005 has been received and its contents carefully considered. Applicants respectfully request reconsideration and allowance of the above-captioned application.

Claims 1-20 remain pending in the application.

In the Office Action, claim 14 is rejected under 35 U.S.C. §102(e) as being anticipated by Prenn et al. Claims 1-3, 6-9, 12 and 13 are rejected under 35 U.S.C. §103(a) over Suh and Prenn. Claims 4-5, 10 and 11 are rejected under 35 U.S.C. §103(a) over the combination of Suh, Prenn and Monahon. Claims 15-20 are rejected under 35 U.S.C. §103(a) over the combination of Prenn and Monahon.

An exemplary embodiment of the features recited in the independent claims is illustrated in Applicants' Figure 3. Figure 3 shows a plurality of interrupt sources 310, namely, IS-01 through IS-K, that are each mapped to a plurality of interrupt inputs, namely, INT-01 through INT-N, that are managed in interrupt controller 340 associated with one or more processors (not shown). The system comprises a plurality of logical mapping subsets, 315-1 through 315-N, each corresponding to one of the interrupt inputs, INT-01 through INT-N. The system 300 is arranged to provide mapping between any of the K interrupt sources 310, IS-01 through IS-K, and any one or more of the interrupt inputs, INT-01 through INT-N, of the interrupt controller 340. An interrupt request from an interrupt source 310, to any one or more interrupt inputs, INT-01 through INT-N, is selectively enabled by setting the value of the corresponding bit in control bit sets that are respectively associated with the interrupt inputs, to enable or disable the receipt of the interrupt request from the

interrupt source 310. For example, in Figure 3, interrupt source IS-02 is mapped to interrupt input INT-01 through logical AND gate 320-2 and logical OR gate 325 by setting control bit 2 of control bit set 01 to enable the receipt of an interrupt request at interrupt input INT-01. Likewise, interrupt source IS-02 is mapped to interrupt input INT-N through logical AND gate 330-2 and logical OR gate 335 by setting control bit 2 of control bit set N to enable the receipt of interrupt request at interrupt input INT-N. Interrupt source IS-02 can be mapped to the rest of the interrupt inputs similarly through the respective other logical mapping subsets.

In contrast, the Suh and Prenn patents deal with specific methods of generating an interrupt vector in response to an interrupt request. Suh's patent is a method to reduce the time it takes to generate the address of the interrupt service routine. Prenn's patent is a method for determining the maximum priority interrupt to service, which is a hardware prioritization scheme.

In paragraph 2, the Office Action identifies Figure 6 of Prenn as disclosing all of the features of claim 14. Claim 14 recites a system for sharing a plurality of interrupt inputs comprising, for each interrupt input, a plurality of logical AND gates, each corresponding to an interrupt source, a plurality of control bits, each corresponding to an interrupt source, and a logical OR gate to indicate, to the interrupt input, the presence of a corresponding interrupt request signal from at least one output of the plurality of logical AND gates. The structure shown in Figure 6 of the Prenn patent does not function to indicate the presence of an interrupt request signal to the interrupt input, as recited in claim 14. Rather, this structure corresponds to the product term generator 252, summary term generator 206, and

selection circuit 208 shown in Figure 2 of the patent. The output of these circuits comprises a maximum value signal MV on line 152. In contrast, the interrupt request signal IRQ that is sent to an interrupt input is produced by the request logic 204. It can be seen from Figure 2 that the circuits 252, 206 and 208 are not involved in the generation of the interrupt request.

Among other distinctions, therefore, the logical OR gates 632-636 in Figure 6 do not indicate "to the interrupt input" the presence of an interrupt request signal, as recited in claim 14. Rather, they each produce a summary term bit ST that is provided to the selector circuit.

In paragraph 4, the Office Action rejects claims 1-3, 6-9, 12 and 13 under Suh and Prenn. The Office Action points to logic structures 30, 40 and 50 in Figure 3 of Suh as teaching all of the features of the claim except for the feature of "selectively enabling interrupt requests from each of the plurality of interrupt sources." The Office Action proposes to modify Suh with Prenn to teach the missing feature.

Firstly, Suh does not disclose mapping each of the plurality of interrupt sources to each of the plurality of interrupt inputs. In making the rejection, the Office Action refers to the parallel connection of the pending register 30 to each of the first priority determination logic 40 and the second determination priority logic 50. The structure of the first priority determination logic 40 is illustrated in Figure 4. The structure of the second priority determination logic is the same (column 5, lines 1-4). As can be seen, these logic circuits have inputs that are dedicated to the interrupt sources in a one-to-one relationship. There is no teaching that "each" of the plurality of interrupt sources is mapped to "each" of the plurality of interrupt inputs.

The Office Action suggests that Suh could be modified by Prenn to provide the "selectively enabling" feature of claim 1. However, that feature is not taught by Prenn, as discussed above. Consequently, any possible combination of the two references does not lead one to the claimed subject matter.

Since Suh and Prenn do not teach all of the features of claims 1, 7 or 14, a discussion of the Monahan patent is believed to be unnecessary at this time.

Should any questions arise in connection with this application, or should the Examiner believe a telephone conference would be helpful in resolving any remaining issues pertaining to this application, the undersigned respectfully requests that he be contacted at the number indicated below.

Respectfully submitted,

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